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09/751,610	12/29/2000	William A. Harris	H16-26054 US	8597

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EXAMINER	
COX, CASSANDRA F	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 10/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,610	HARRIS, WILLIAM A.	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,20 and 21-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 20-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *14* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Applicant's arguments filed 06/20/03 have been fully considered but they are not persuasive. Therefore, the rejection is repeated below.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 20, 22, 23, 25, 27, 28, 30, 32, 35, 36, 38, 40, 43, 44, and 46 are rejected under 35 U.S.C. 102(b) as being anticipated by Moreau (U.S. Patent No. 4,282,493).

In reference to claim 1, Moreau discloses in Figures 2 and 5, a circuit for dividing an input clock signal into N clock signals having a relative phase separation of 360°/2N, where N is a positive integer, the circuit comprising: a phase lock loop circuit (201) receiving an input signal having a frequency F_0 and providing an output signal (the output of level converter 206) having a frequency $2NF_0$; and a Johnson counter (207) having N stages connected to receive as an input the output signal (the output of level converter 206) of the phase lock loop circuit and providing an output signal (OUTPUT A, OUTPUT B; Fig. 5) as an error signal to the phase lock loop circuit (the output of 207); the Johnson counter (207) also connected for providing at least two output signals (OUTPUT A, OUTPUT B; Fig. 5) from at least two of the N stages of the Johnson

counter (207) as clock signals each having a phase displaced from the phase of the other 360°/2N (column 7, lines 23-27). The same applies to claims 20, 22, 23, 27, 28, 32, 35, 36, 40, 43, and 44.

In reference to claim 25, Moreau discloses in Figure 5 wherein the Johnson counter (207) comprises a shift register having N stages (2) including an input stage (501) and an output stage (502), a complement of a state of the output stage being coupled to a serial input of the input stage (which is seen as the inverted version of the Q output being applied to the K input), each stage of the Johnson counter (207) being coupled to provide a clock signal (OUTPUT A, OUTPUT B), the N (2) clock signals having a relative phase separation of at least 360/2N, and each clock signal having a frequency F_0. The same applies to claims 30, 38 and 46.

4. Claims 1, 20, 24, 29, 32, 37, 40, and 45 are rejected under 35 U.S.C. 102(b) as being anticipated by Li et al. (U.S. Patent No. 5,058,132).

In reference to claim 1, Li discloses in Figure 2, a circuit (100) for dividing an input clock signal in to N clock signals having a relative phase separation of 360/2N, where N is a positive integer, the circuit comprising: a phase lock loop circuit (102) receiving the an input signal (116) having a frequency F_0 and providing an output signal (124) having a frequency $2NF_0$; a Johnson counter (114) having N stages connected to receive as an input the output signal (124) of the phase lock loop circuit (102) and providing an output signal (LBC1-5) as an error signal to the phase lock loop circuit (column 5, lines 25-28); and the Johnson counter (114) also connected for providing at least two output signals (LBC1-LBC5) from at least two of the N stages of the Johnson

counter (114) as clock signals each having a phase displaced from the phase of the other 360/2N. The same applies to claims 20, 32, and 40.

In reference to claim 24, Li discloses in Figure 2, wherein the phase lock loop circuit (102) comprises: a phase detector (104) coupled to receive and compare the input signal (116) having a frequency F_0 and the error signal (123) from the Johnson counter (114) and providing an output signal (121) corresponding to the phase difference between the input clock signal (116) and the error signal (123); a low pass filter and gain stage (106) coupled to receive the output signal from the phase detector (104) and producing a control signal (125); a voltage controlled oscillator (108) coupled to the low pass filter and gain stage (106) to receive the control signal and coupled to the Johnson counter (114) to produce the output signal (124) having the frequency $2NF_0$ in response to the control signal (125. The same applies to claims 24, 29, 37, and 45.

5. Claims 1, 20, 24, 29, 32, 37, 40, and 45 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujii (U.S. Patent No. 5,315,269).

In reference to claim 1, Fujii discloses in Figures 6-7, a circuit for dividing an input clock signal in to N clock signals having a relative phase separation of 360/2N, where N is a positive integer, the circuit comprising: a phase lock loop circuit (101, 102, 103) receiving the input signal (61-64) having a frequency F_0 and providing an output signal (OUT) having a frequency $2NF_0$; a Johnson counter (105) having N stages connected to receive as an input the output signal (OUT) of the phase lock loop circuit (101, 102, 103) and providing an output signal (71-74) as an error signal to the phase

lock loop circuit; and the Johnson counter (105) also connected for providing at least two output signals (71-74) from at least two of the N stages of the Johnson counter (105) as clock signals each having a phase displaced from the phase of the other 360/2N. The same applies to claims 20, 32, and 40.

In reference to claim 24, Fujii discloses in Figure 7, wherein the phase lock loop circuit comprises: a phase detector (11-14) coupled to receive and compare the input signal (61-64) having a frequency F_0 and the error signal (71-74) from the Johnson counter (105) and providing an output signal (OUT) corresponding to the phase difference between the input clock signal (61-64) and the error signal (71-74); a low pass filter and gain stage (106, 107, 102) coupled to receive the output signal from the phase detector (11-14) and producing a control signal; a voltage controlled oscillator (103) coupled to the low pass filter and gain stage (106, 107, 102) to receive the control signal and coupled to the Johnson counter (105) to produce the output signal (OUT) having the frequency $2NF_0$ in response to the control signal. The same applies to claims 24, 29, 37, and 45.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-3, 21, 33-34, and 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moreau (U.S. Patent No. 4,282,493).

In reference to claim 2, Moreau discloses all of the limitations of the claim as mentioned above with reference to claim 1, except that Moreau does not disclose that N is equal to 4. However, this is seen to be a design expedient dependent on the particular environment. Therefore, it would have been obvious to one of ordinary skill in the art that the value of N could be any number including 4, dependent on the particular environment and the desired results of the circuit. The same applies to claims 3, 21, 33-34, and 41-42.

8. Claims 26, 31, 39, and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. (U.S. Patent No. 5,058,132) in view of Epstein (U.S. Patent No. 4,093,870).

In reference to claim 26, Li discloses all the limitations as mention above with respect to claim 1 except Lid does not disclose the particular design of the Johnson counter as called for in claim 26. Epstein discloses in Figure 4 a Johnson counter comprising N JK flip-flops (182, 184, 186) comprising an input JK flip-flop (186), an output JK flip-flop (182), and a plurality of middle JK flip-flops (184; while only one fiddle flip-flop is shown it is considered to be well known that you could have any number of middle flip-flops depending on the requirements of the circuit), each JK flip-flop having a J input, a K input, a clock input coupled to receive the output signal having the frequency $2NF_0$ from the phase locked loop circuit (this is seen as the T input), a Q output, and a complemented Q output, each middle JK flip-flop and the output JK flip-

flop having its J input coupled to the Q output of a preceding JK flip-flop and its K input coupled to the complemented Q output of the preceding JK flip-flop, the J input of the input JK flip-flop (186) being coupled to the Q output of the output JK flip-flop (182), the K input of the input flip-flop (186) being coupled to the Q output of the output JK flip-flop (182), and each Q output and each complemented Q output of each JK flip-flop being coupled to provide a clock signal, the 2N clock signals having a relative phase separation of 360/2N, and each clock signal having a frequency F_0. It would have been obvious to one skilled in the art at the time of the invention that the Johnson counter of Epstein could be used as the Johnson counter in the circuit of Li. Since, Li does not disclose the particular construction of the Johnson counter any Johnson counter could be used and the Johnson counter of Epstein is one example. The same applies to claims 31, 39, and 47.

Response to Arguments

9. Applicant's arguments filed 06/20/03 have been fully considered but they are not persuasive. Applicant's argument that the Moreau patent does not disclose a proper Johnson counter is not persuasive. The Moreau reference shows in Figure 5 that the input K of flip-flop 501 receives the inverted version of the Q output of flip-flop 502.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 703-306-5735. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:30 PM and on alternate Fridays from 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703)-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

CC

September 22, 2003

TIMOTHY P. CALLAHAN
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